REMARKS

Claims 1-22 are pending in the application.

Claims 1-22 had been rejected.

Reconsideration of the Claims is respectfully requested.

Applicant notes with appreciation the Examiner's consideration of its Response of June 9, 2005 to the Office Action dated March 9, 2005.

1. Rejection under 35 USC § 103(a)

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142, p. 2100-128 (Rev. 2, May 2004) (citations omitted).

a. Claims 1-12, 16-19 and 22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Auckland et al (US Pub 20020183013) and in view of Loyer (US 4652874). Applicant respectfully traverses this rejection.

Auckland relates to an "analog RF hardware in the front ends of personal and mobile communication radios that is reconfigurable for a variety of air interface standards." (Auckland ¶ 0048). In this regard, Auckland generally recites memory in an operational usage for RF portion 600 configurations, which includes a "controller 614 may be dedicated to controlling the RF front end of the radio, including functions such as modulation, demodulation, encoding and decoding. In a software definable radio, where the radio hardware is fixed but may be customized by on-board software during operation to allow the radio to operate in conjunction with a particular air interface standard or on a particular frequency band, the customization operation may be controlled by the controller 614." (Auckland ¶¶ 0077, 0090; *see* Figure 6).

Loyer relates to a "serial communications interface which connects the physical layer to the media access control layer of a local area network [(LAN)]. The serial communications interface of the present invention is utilized to transfer serial data to and from a [LAN] controller . . . ." (Loyer 1:9-16).

The Token Bus Controller (TBC) 10 of Loyer recites "a 32-byte FIFO 18 [that] is provided for message buffering." (Loyer 5:46-48; *see also* 5:55-59). Figure 6 of Loyer provides an "initialization table [that] contains pointers to the head of each queue, 8 pointers in all. In reality the receive queue pointers are both the 'head' and the 'tail' of the queue because the queue is a null set at initialization." (Loyer 9:29-53). These pointers are statically configured in the initialization table of Figure 6 for an Ethernet Token Bus Controller for use on device initialization. That is, the initialization table of Loyer does not serve as a FIFO.

In contrast, taken in context, Applicant's invention of Independent Claim 1 recites, *inter alia*, a "wireless transceiver device, comprising: modulation circuitry for modulating and demodulating signals that are transmitted over the airwaves; . . . baseband processing circuitry including a first in, first out memory structure for storing addresses for accessing data blocks." (emphasis added).

Independent Claim 7 recites a "method for storing and transmitting data, comprising: storing a data block in random access memory; and storing a pointer that corresponds to the data block in a first in, first out memory structure."

Independent Claim 17 recites a "memory structure formed within a baseband processing system, comprising: a random access memory portion for storing data blocks that are to be transmitted in a first in, first out order; and a first in, first out memory structure for storing pointers that correspond to the data blocks."

As explained at page 14 of Applicant's specification, "FIFO memory structure 242 is for controlling and providing access to actual data blocks that are stored within random access memory portion 246 in a manner that causes the data blocks to be transmitted in a first in, first out basis without requiring the data to actually be stored within the FIFO memory structure 242." (Specification at p. 14, *ll.* 12-17).

Applicant respectfully submits that a *prima facie* case of obviousness has not been established. There is no suggestion or motivation in the configurable RF front-end of Auckland or in the LAN token bus controller of Loyer to achieve Applicant's claimed invention. Further, the hypothetical combination of Auckland with Loyer does not teach or suggest all the claim limitations of Applicant's wireless transceiver device of Claim 1, its method for storing and transmitting data of Claim 7, and its memory structure of Claim 17. The lack of suggestion or motivation may not be created by relying on elements

individually known in the art without some objective reason to combine the teachings of the references. MPEP § 2143.01 at p. 2100-131 (Rev. 2, May 2004). Accordingly, Applicant respectfully submits that its Claim 1 and Claims 2-6 that depend directly or indirectly therefrom, its Claim 7 and Claims 8-12 and 16 that depend directly or indirectly therefrom, and its Claim 17 and Claims 18-20 and 22 that depend directly or indirectly therefrom are allowable.

b. Claims 13-15 and 20-21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Auckland and in view of Loyer and further in view of Firoozmand (US 5136582).

Claims 13-15 depend indirectly from Claim 7. Claims 20 and 21 depend indirectly from Claim 17. In this regard, because a *prima facie* case of obviousness was not established to Independent Claims 7 and 17, Applicant submits that there is no suggestion or motivation to combine Auckland with Loyer and further in view of Firoozmand as set out in the Office Action. Accordingly, Applicant respectfully submits that Claims 13-15 and Claims 20 and 21 are allowable.

2. Conclusion

As a result of the foregoing, the Applicant respectfully submits that Claims 1-22 in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *ksmith@texaspatents.com.*

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Garlick Harrison & Markison Deposit Account No. 50-2126 (BP1907).

Respectfully submitted,

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